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SACLANT ASW
RESEARCH CENTRE

A DIGITAL DEPTH RECORDER

by

A. JOHANSEN

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A DIGITAL DEPTH RECORDER

By

A. Johansen

ABSTRACT

The depth recorder described has been designed for the direct computer processing of data, which it provides in digital form on perforated tape. It is intended as a supplement to the Precision Depth Recorder installed on the Centre's Research Vessel.

INTRODUCTION

The amount of oceanographic data collected is growing rapidly year by year. Usually these data are collected by means of analogue recorders that have to be read out afterwards. Then the data, thus read out, have to be converted into a form that can be accepted by a digital computer in order to be processed.

As the read-out and converting processes are tedious and time consuming, SACLANTCEN decided to supplement the analogue recorders by digital recorders. In this way the data would be punched out on paper tape as soon as they were measured, and the perforated tape could be processed by the computer directly.

One of the instruments that SACLANTCEN decided to supplement by a digital recorder was the Precision Depth Recorder. A description of how this digitalization was carried out is the subject of this report.

1. DESIGN CONSIDERATIONS AND PRELIMINARY TRIALS

1.1 Basic Specifications

In principle, a digital depth recorder (hereafter referred to as DDR) is quite simple, as indicated in the block diagram of Fig. 1. The transmission of the echo-sounding pulse starts an electronic counter that is stopped when the bottom echo returns. The output of the counter is connected to a punch, thus permitting the reading to be perforated on paper tape.

The problem is to discriminate the bottom echo from background noise (caused by the ship, waves, etc.), echoes from fish and other scatterers, and from pulses emitted by other sounding systems simultaneously in use aboard the research vessel. To carry out this discrimination it was considered necessary to take the following measures:

a. To use an amplifier with time-variable gain in the receiving channel. The gain should increase with time after each transmission of the Echo Sounder, thus suppressing the comparatively weak echoes from shallow fish and scattering layers. This measure would also make the DDR more automatic, as gain adjustment of the Echo Sounder would hardly be necessary.

b. To use a coded transmission instead of the conventional single sound pulse. The receiving system should be so constructed that it would only admit the coded echoes, thus almost eliminating

the possibility that background noise or pulses from other sounding systems would operate the DDR.

c. To be able to control the stop of the electronic counter during severe background noise conditions (as for example during a storm). Under such conditions it should only be possible to stop the counter during a short time interval occurring around the expected time of arrival of the bottom echo.

d. To further reduce interference with other sonar equipment aboard the ship by using a separate working frequency for the DDR Echo Sounder.

1.2 Choice of gain/time ratio for variable-gain amplifier

In order to find the desired relationship between gain and time for the variable gain amplifier (para 1.1a), the sound propagation losses have been calculated. The approximate total propagation losses at 15 kHz and relative to a depth of 100 fm are given in Table 1. It was considered practical to specify that no gain adjustment of the Echo Sounder should be necessary for depths between 100 and 2000 fm, and therefore that the gain of the amplifier ought to increase with time in approximately the same way as the losses.

TABLE I

TOTAL RELATIVE PROPAGATION LOSS AT 15 kHz vs DEPTH AND TIME					
Depth in fm	100	500	1000	1500	2000
Relative prop. loss in dB	0	19	31	41	49
Corresponding time in seconds	0.25	1.25	2.5	3.75	5.0

1.3 Choice of echo code

Preliminary sea trials were carried out in order to determine a suitable code for the coded transmission (para 1.1b). The following four codes were tried:

1. One 50 ms long pulse (the pulse length of our Echo Sounders is normally 5 ms or less).

2. Two pulses, each 50 ms long, transmitted with an interval of 100 ms in between.

3. Two 4-ms pulses transmitted with an interval of 146 ms in between.

4. Three 4-ms pulses transmitted with intervals of 146 ms in between.

All four codes appeared to give reasonably good protection against noise and pulses from other Echo Sounders, but the depth-measuring

accuracies were found to be widely different. When using code 1 the discrimination process was an integration of the received signals, the integration time being about 30 ms. In order to avoid accumulation of noise signals in the integration capacitor, the latter was automatically short-circuited if the signal level dropped below a certain, prefixed value. Thus, if the level of an echo pulse dropped below this value during the first 25 ms of its appearance, the integration process would start all over again. Due to this, inaccuracies of up to 10 fm were experienced.

The same thing happened when code 2 was tried. Here the discrimination process was a combination of integration and pulse delay.

Codes 3 and 4 proved to give accuracies of the order of 1 fm. The discrimination process was in both cases a combination of integration and pulse delay, but no automatic discharging of the integration capacitor was used. The integration time was 1 ms.

As a result of the trials it was decided to use code 3, because this was the simplest code giving both good accuracy and good protection against unwanted signals.

1.4 Choice of stop-control for electronic counter

Several ways of controlling the stop of the electronic counter during severe background noise conditions (para 1.1c) have been considered. One was to equip the DDR with a memory (of the last reading) and let this memory open a signal gate shortly before the return of the next bottom echo.

This system would probably work well if it was not for the occasional lack of bottom echoes when passing over a bottom with big slopes. During such periods the bottom echo might travel outside the gating pulse generated by the memory. Of course the memory unit could be designed to widen the gating pulse or to go searching once the bottom echo was lost. However, it was felt that this might complicate the DDR unnecessarily. Therefore, it was decided to use a simpler system utilizing a generator that could create a gating pulse of adjustable width at a manually selectable time after the sound-pulse transmission. During periods with low noise the gating pulse could be set wide, thus permitting the DDR to operate automatically over a wide range of depth, but under high noise conditions a narrow gating pulse, needing readjustment from time to time, would be used.

1.5 Choice of frequency

A working frequency of 15 kHz was chosen for the DDR Echo Sounder because no other sonar equipment aboard our ship used this frequency and because, not being too far from the 12 kHz of the standard echo-sounder, attenuation losses would not be greatly increased.

2. GENERAL DESCRIPTION

A simplified block diagram demonstrating the working principle of the DDR is shown on Fig. 1. When triggered, the Double-Pulse Generator generates two 4-ms wide, 150-ms spaced pulses. The first pulse is fed to the Reset Circuit, thus resetting all bi-stable elements of the DDR; the second pulse reverses the start/stop flip-flop that in turn starts the counter counting the 400 pps from the oscillator.

Both pulses are fed to the Transmitter of the Echo Sounder, thus causing two sound pulses to be transmitted into the water. A little later the two corresponding echoes are received and, after being filtered, are amplified and shaped, and fed simultaneously to the 150-ms Delay Circuit and the And-Gate (B). The first echo pulse, being unable to pass through this Gate, travels through the Delay Circuit and arrives at the input of the Gate at the same time as the second echo pulse appears at the output of the receiver. Provided that the variable-delay gating voltage for protection during severe noise conditions (para 1.5) is present, the second echo pulse will pass the And-Gate (B) and reverse the Start/Stop flip-flop, thus closing the And-Gate (A). Consequently, the Counter stops after having counted the number of pulses occurring during the time period from the transmission of the second sound pulse to the reception of the corresponding bottom echo. A counting frequency of 400 pps has been chosen in order to have the uncorrected depth-grading directly in fathoms (the speed of sound in sea water is about 800 fm/s and the sound has to travel to the bottom and up to the ship again).

As the flip-flop is reversed to its "stop" position, the Scanner Command circuit is triggered and makes the Scanner successively connect the four decade counters (of the Frequency Counter) to the Punch. The Scanner Command also gives the punching orders to the punch. As soon as the data are punched on the paper tape the DDR is ready for a new cycle. The repetition rates selected for the DDR are 10 sec, 30 sec, 1 min, and 5 min.

The variable delay is achieved by connecting a number of And-Gates to the Counter by means of three selector switches. The selector switches have settings graded in fathoms, the biggest increment being 1000 fm and the smallest 10 fm. The output from the And-Gates triggers the Gating Voltage Generator. The width of the gating voltage is also controlled by a selector switch with settings ranging from 10 to 1000 fathoms. There is also a setting where the gating voltage will be present until the next reset appears.

Some waveforms from the DDR are given in Fig. 2. From the top, the waveforms shown are:

The output of the Double Pulse Generator.
The output of the Echo Sounder Receiver.
The inputs of And-Gate (B): the shaped signal,
the delayed signal,
the variable gating voltage.
The detected signal on the output of And-Gate (B).
The inputs of And-Gate (A): the flip-flop output,
the 400 cps from the oscillator.
The input of the Frequency Counter.

Figure 3 gives a more detailed block diagram of the DDR showing a few features not mentioned before.

The DDR is controlled from a Digital Clock delivering the 400 pps counting frequency and the 1 pps repetition-rate frequency that is subdivided in the Repetition Rate Divider and Selector to give the above mentioned repetition rates of 10 sec, 30 sec, 1 min, and 5 min.

The Digital Clock also has outputs giving the exact time in digital form. These outputs are connected as shown to the Electronic Scanner, which actually has sixteen positions, the first one giving a time symbol, the next ten giving the time, the twelvth giving a depth reading symbol, and the last four giving the depth. On the output of the Scanner is a Parity Bit Generator checking the parity of the four data levels.

The time is not punched with each depth reading because this would result in an unnecessarily high paper-tape consumption. Instead, the repetition rate is contained in the depth-reading symbol and is thus perforated on the tape so that the computer can keep track of the time. Every hour the Digital Clock delivers a pulse to the Scanner Command Circuit, causing it to punch the time together with the next depth reading. There is also a connection to the Scanner Command from the Repetition Rate Divider and Selector, causing the time to be punched when the repetition rate is changed. The repetition rate selector, apart from triggering the Double-Pulse Generator, also synchronizes the Exponential Waveform Generator, which again varies the gain of the Time-Variable Gain Amplifier.

Sometimes the amplitude of the received echo pulses is not large enough to trigger the Pulse Shaper. In this case the Frequency Counter will go on until the count is 3000. At this count the And-Gate (C) will open and the pulse thus generated will pass through the Or-Gate and reverse the Start/Stop Flip-Flop. Consequently the reading of the counter will be 3000 fathoms and the computer will be instructed to regard this as "No echo received".

Four Nixie tubes with decoders are connected to the Counter and visually display the depth in fathoms.

A photograph of the actual DDR is shown on Fig. 4. The upper panel contains the electronic circuitry, the display tubes, and the Repetition Rate Delay, Gate Width, and Gain controls. The next panel contains the Punch with its driver cards and the bottom panel contains the power supplies.

Printed circuit cards have been used throughout, and the logic components are Philips Circuit Blocks.

3. DETAILED DESCRIPTION

A complete wiring diagram of the DDR is shown in Fig. 5. The following brief descriptions of the sub-units refer to this wiring diagram, if not otherwise stated. The terminology of Fig. 3 for the sub-units will be used when practical.

3.1 Repetition Rate Divider (Cards 1 & 2 and Panel)

This consists of a 1 Hz unijunction transistor oscillator followed by an amplifier, a pulse shaper, ten flip-flops, and the repetition rate selector switch S1. The latter is located on the front panel. The flip-flops divide down the shaped one-second pulses to give the desired repetition rates (10 sec, 30 sec, 1 min, 5 min). The four divider outputs are connected to wafer (e) of S1, the centre contact of which is fed to the input of the Double-Pulse Generator (Card 4). Wafers(a), (b), and (c) of S2 are used to feed the repetition rate symbols to the Scanner, and wafer (d) is used to give the "Punch Time" order to the Scanner Command Circuit when the repetition rate is changed. The Repetition Rate Divider may also be driven from an external source by changing the position of switch S7.

3.2 Double-Pulse Generator (Card 4) and Transmitter Triggering Circuit (Card 39)

The Double Pulse Generator consists of a one-shot multivibrator, a delay circuit (formed by a flip-flop, a switching transistor, and

a unijunction transistor), a second one-shot multivibrator, and an Or-Gate. When triggered, the first one-shot multivibrator emits a 4-ms pulse and simultaneously starts the delay circuit by reversing the flip-flop. 150 ms later the delay circuit delivers an output pulse, simultaneously resetting the flip-flop and triggering the second one-shot multivibrator.

The two pulses thus generated, each 4 ms long and 150 ms spaced, are fed through the Or-Gate into the Transmitter Triggering Circuit. This consists of a pulse shaper and a switching transistor. The internal resistance of the switching transistor becomes low when the 4 ms pulses appear at its base, thus triggering the Echo Sounder transmitter.

3.3 Exponential Waveform Generator (Card 39)

Every 10 sec this generator is synchronized by a pulse from Card 1 of the Repetition Rate Divider (para 3.1). After having passed the input amplifier T1, the synchronizing pulse causes the unijunction transistor to fire, thus discharging the 15 μF capacitor. The latter will start charging again through the transistor (BCZ11), and part of the charging current will be picked up by the current amplifier T2, T3, T4. By means of the 10 kΩ feedback resistor the charging of the 15 μF capacitor will be speeded up as the voltage across it increases, thus causing a voltage with an approximately exponential waveform to appear at the emitter of T4.

The unsynchronized (or natural) period of the Waveform Generator is about 11 sec.

3.4 Amplifier with Time Variable Gain (Card 38) and Pulse Shaper (Card 39)

The signal from the receiver passes a 4-kHz filter, a volume control, and an emitter follower, T1, and is then fed to the base of the variable gain stage, T2. The gain of this stage is controlled by T3, which in turn is driven by the Exponential Waveform Generator described in para 3.3. The output of the transformer-secondary is amplified in T4, and then rectified and filtered in the emitter-follower stage. The rectified signal is fed to the Pulse Shaper located on Card 39 and is, after amplification and inversion, ready to be fed to the Delay Circuit (para 3.5) and to the And-Gate (B) (para 3.6).

3.5 Delay Circuit (Cards 6, 7, 8, 9, 10)

This circuit consists of 30 one-shot multivibrators coupled in series, each giving a delay of 5 ms. The unit is triggered by the shaped signal and will deliver, 145 ms later, a 10 ms wide gating pulse which is fed to the And-Gate (B) (para 3.6).

3.6 AND/OR gates and START/STOP flip-flop (Card 11)

The 2.2N1 at the bottom of the diagram is the And-Gate (B), which is followed by two diodes (OA 200) forming an Or-Gate. The output of the Or-Gate is inverted and fed to the STOP input of the Start/Stop flip-flop, the Start input of which is connected to the Double Pulse Generator (para 3.2). The output of this flip-flop

is simultaneously fed both to a one-shot multivibrator that gives the Start-Scan order to the Scanner Command Circuit (para 3.9), and to the And-Gate (A) that occupies one half of the 2.2N1. The other input of this gate receives the amplified 400 pps counting frequency. The other half of the 2.2N1 forms the And-Gate (C) that stops the counter when the reading is 3000.

3.7 Frequency Counter (Cards 12, 13, 14, & 15)

Each card contains a normal, feedback-type, binary-coded decimal counter, utilizing the 8421 code. The counting frequency is supplied from Card 11 (para 3.6), and the outputs are connected to Cards 27, 28, 29, & 30 of the Scanner (para 3.9), to Switches S2, S3, & S4 of the Variable Delay Selector (para 3.11), to the Display Decoders (para 3.8), and to the And-Gate (C) (para 3.6).

3.8 Display

The Display is located on the front panel and consists of four type 8422 Nixie tubes with type BIP-8211P decoders. The decoders are connected to the bit and the complement outputs of the Frequency Counter (para 3.8).

3.9 Scanner and Scanner Command Circuits

The Scanner is located on Cards 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, and 36, and the Scanner Command on Cards 3, 5, and 17.

The Scanner has sixteen positions: A, B, C, D, E, F, G, H, I, J, K, L, P, O, N, M, that are scanned in the given order. The information to be punched is connected to the And-Gates of these sixteen positions in the following manner:

Position	A	: Time Reading Symbol
"	B	: Tens of Months
"	C	: Units " "
"	D	: Tens of Days
"	E	: Units " "
"	F	: Tens of hours
"	G	: Units " "
"	H	: Tens of Minutes
"	I	: Units " "
"	J	: Tens of seconds
"	K	: Units " "
"	L	: Depth Reading and Repetition Rate Symbol
"	P	: Thousands of fathoms
"	O	: Hundreds of fathoms
"	N	: Tens of fathoms
"	M	: Units of fathoms

(The punch code used is given in the Appendix).

The And-Gates of the sixteen Scanner positions (Cards 20 to 30) are controlled by sixteen flip-flops. When one of the latter is reversed, the corresponding gates open, thereby connecting the informations on their inputs to the punch through the Or-Gates and Amplifiers on Cards 31, 33, 34, 35, and 36. The reversing of the

flip-flop also causes a punching-order pulse to be sent to the punch via the Or-Gates, pulse-shapers, one-shots, and amplifiers of Cards 18, 19, and 32. The Punch now punches out the data. This process is completed in about 45 ms.

The punching-order pulse also enters into Card 17 of the Scanner Command Circuit where it triggers a delay circuit similar to the one described in para 3.2. About 60 ms later the delay circuit generates a pulse that, after passing through one side of the And-Gate located on Card 17 and one of the amplifiers on Card 5, resets the reversed flip-flop, thus closing the And-Gates that contain the information just punched.

When this flip-flop is reset to its original state, it triggers the flip-flop of the succeeding position, which in turn connects the information of this position to the punch, and triggers the Punch and the Scanner Command Circuit. It thus takes 45 ms for the punching process to be completed, so that there is a gap of 15 ms before the pulse resetting the now reversed flip-flop is generated by the delay circuit. The Scanner Command has separate reset lines for the odd (A, C, E, G, I, K, P, N) and even (B, D, F, H, J, L, O, M) scanner positions. This is to avoid the flip-flops from receiving a reversing and a resetting pulse simultaneously. The second flip-flop on Card 17, by means of the succeeding And-Gate, shifts the reset pulse from one reset link to the other.

Normally only the last five Scanner positions (L, P, O, N, M) are punched. The scanning is initiated when the Start/Stop flip-flop

on Card **11** (para 3.6) is reversed by the returning echoes. The succeeding one-shot multivibrator is thereby triggered and its output pulse is fed to the double And-Gate of the Scanner Command (Card 3). This And-Gate is controlled by the preceding flip-flop, which usually directs the pulse through the right-hand side of the gate to the pulse-shaper and one-shot on Card 26. The one-shot in turn reverses the flip-flop, thus connecting the Depth and Repetition Rate Symbol of position L to the punch. Thereafter, positions P, O, N, and M (and thereby the four decade counters) are connected successively to the punch, and the depth data are punched out as explained above. When the punching of position M is completed, all flip-flops are reset and the Scanner stops.

When the repetition rate is changed, the "Punch-Time" push-button (S10) pressed, or an hour pulse arrives from an external clock (via plug PLA), the flip-flop on Card 3 is reversed by the one-shot and pulse-shaper on the same Card. Thus, next time that a pulse from the one-shot on Card **11** arrives, it is directed through the left side of the double And-Gate (Card 3), and, after having passed the pulse-shaper and one-shot on Card 20, reverses the flip-flop of position A. In this case all sixteen positions will be scanned and the time and depth punched.

The output pulse of the one-shot on Card 20 sets the flip-flop on Card **17** to such a position that, when all sixteen positions are punched, the first reset pulse is directed to the flip-flops of the odd Scanner positions (A, C, E, G, I, K, P, N). The flip-flop of Scanner position F also resets the flip-flop on Card 3. Thus, on the following scans, only the five depth positions will be read.

3.10 Parity Bit Generator (Card 37)

This unit consists of three half-adders. Two of these check the four data levels (two levels each) and the third checks the outputs of the first two.

The output of the Parity Bit Generator is connected to the fifth level of the Punch and causes a hole to be punched when the parity of the four data levels is even. The sixth level is punched permanently, and thus the parity of the complete tape becomes even. Sometimes the seventh and eighth levels are also punched (for the time and depth symbol), but always together. Consequently they do not change the even parity.

3.11 Variable Delay Selector (Card 16 and Panel)

This sub-unit consists of a twelve-input And-Gate and an inverter amplifier located on Card 16, and three 4-wafer, 10-position switches (S2, S3, and S4) placed on the front panel. The contacts of these switches are connected to the bit and the complement outputs of the decimal counters on Cards 13, 14 and 15 (para 3.7), and the contact arms are connected to the twelve-input And-Gate. Thus, a pulse is produced at the output of the gate at a pre-selected time after each transmission. The switches are graded in fathoms and may be set, in steps of 10 fm, to any depth between 0 and 9990 fm.

The output pulse of the And-Gate is amplified, inverted, and fed to the Gating Voltage Generator (para 3.12).

3.12 Gating Voltage Generator (Card 16 and Panel)

This generator consists of a flip-flop, a switching transistor, and a unijunction transistor circuit located on Card 16, and an eight-position switch located on the front panel.

When triggered, it operates in the same way as the delay circuit described in paragraph 3.2. The generated gating voltage is taken from the flip-flop and fed to the three-input And-Gate on Card 11 (para 3.6).

The duration of the gating voltage is changed by inserting resistors with different values in the RC-circuit of the unijunction transistor. This is done by means of the switch S5, the positions of which are graded in fathoms.

3.13 Reset Circuit (Card 5)

This circuit consists of an emitter follower, a switching transistor, and a double-inverter amplifier (the two remaining double-inverter amplifiers on this card are parts of the Scanner Command Circuit). The Reset Circuit is triggered by the first pulse from the Double Pulse Generator (para 3.2). The emitter-follower and the switching transistor then reset the sixteen flip-flops of the Scanner (para 3.9) and the double-inverter amplifier resets all other flip-flops.

3.14 Punch Control (Panel)

The punch is controlled by the 4-wafer, 3-position switch S8 and the push-button S9, both located on the front panel. With S8 in position 1 the Punch is connected to, and controlled by, the Scanner (para 3.9); in position 2 it is disconnected from the Scanner, and a feedback loop is formed from the last to the first one-shot of the Punch's sequencer card. Simultaneously, punch levels 5 and 6 are connected to -12V in order to prevent holes from being punched. Thus, the punch advances continuously without punching.

With S8 in position 3, the feedback loop is broken and the punch will only advance one step each time S9 is pushed.

3.15 Power Supply

The power supply is located in a separate rack-mounted cabinet. It consists of two modular power supplies from Contant Electronics Ltd., U.K., and a regulated power supply with outputs for +200V dc, +6V dc, and -12V dc, as shown in the circuit diagram of Fig. 7.

The ED 200 modular power supply gives +6V and -6V to the logic circuitry of the DDR, and the D 100 gives -26V to the solenoids of the punch.

The combined power supply gives +200V to the Nixie Tubes, -12V to the output amplifiers of the Scanner, and +6V to the punch.

4. PERFORMANCE

The DDR was installed aboard MARIA PAOLINA in September 1965. Unfortunately it was not used much during our winter cruises, and it is therefore impossible to give any extensive performance data. However, during a trial cruise in September 1965, in water depths down to 400 fm, it appeared to perform well. A computer analysis of the punched tape showed that it never printed a false depth, and that only about 4% of the echo returns were either missing or were too weak to trigger the input pulse shaper (thus causing 3000 ["echo-missing"] to be punched).

Part of this punched tape was processed by the computer and a record of the area drawn by the X-Y plotter corresponded very well with a depth-profile taken simultaneously with the Precision Depth Recorder.

The maximum depth the DDR can record is 2999 fm (but this may easily be extended) and the resolution of the DDR itself is one fathom.

Measurements of gain versus time on the Amplifier with Time Variable Gain gave the results shown in Table 2. These results compare quite well with the total relative propagation losses given in Table 1 (para 1.2), which are repeated below for comparison.

---

* Since the original manuscript was prepared the DDR has been operated successfully down to depths of 2500 fm.

TABLE 2

RELATIVE GAIN vs TIME OF THE TVG AMPLIFIER COMPARED WITH THE TOTAL RELATIVE PROPAGATION LOSS

Time in seconds	0.25	1.25	2.5	3.75	5.0	
Gain in dB	0	20	33	43	50	
Rel.prop.loss in dB (from Table 1)	0	19	31	41	49	

CONCLUSIONS

The Digital Depth Recorder describes has appeared to work well. In its present form it is controlled by an external electronic clock and has been constructed to work together with the EDO model AN/UQN-IE Echo Sounder, but it could be modified to work with other equipment.

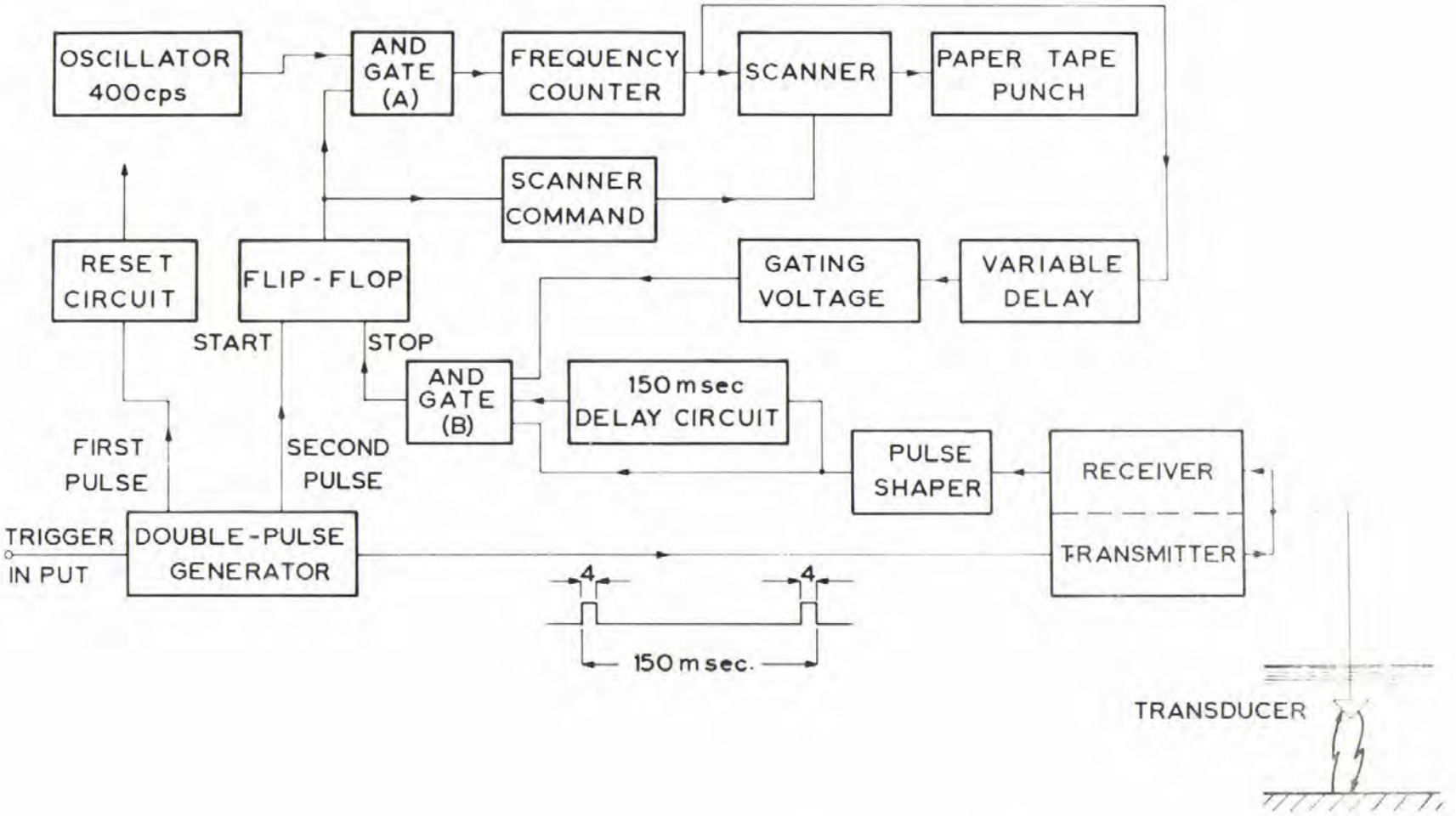


FIG. 1 SIMPLIFIED BLOCK DIAGRAM OF DIGITAL DEPTH RECORDER

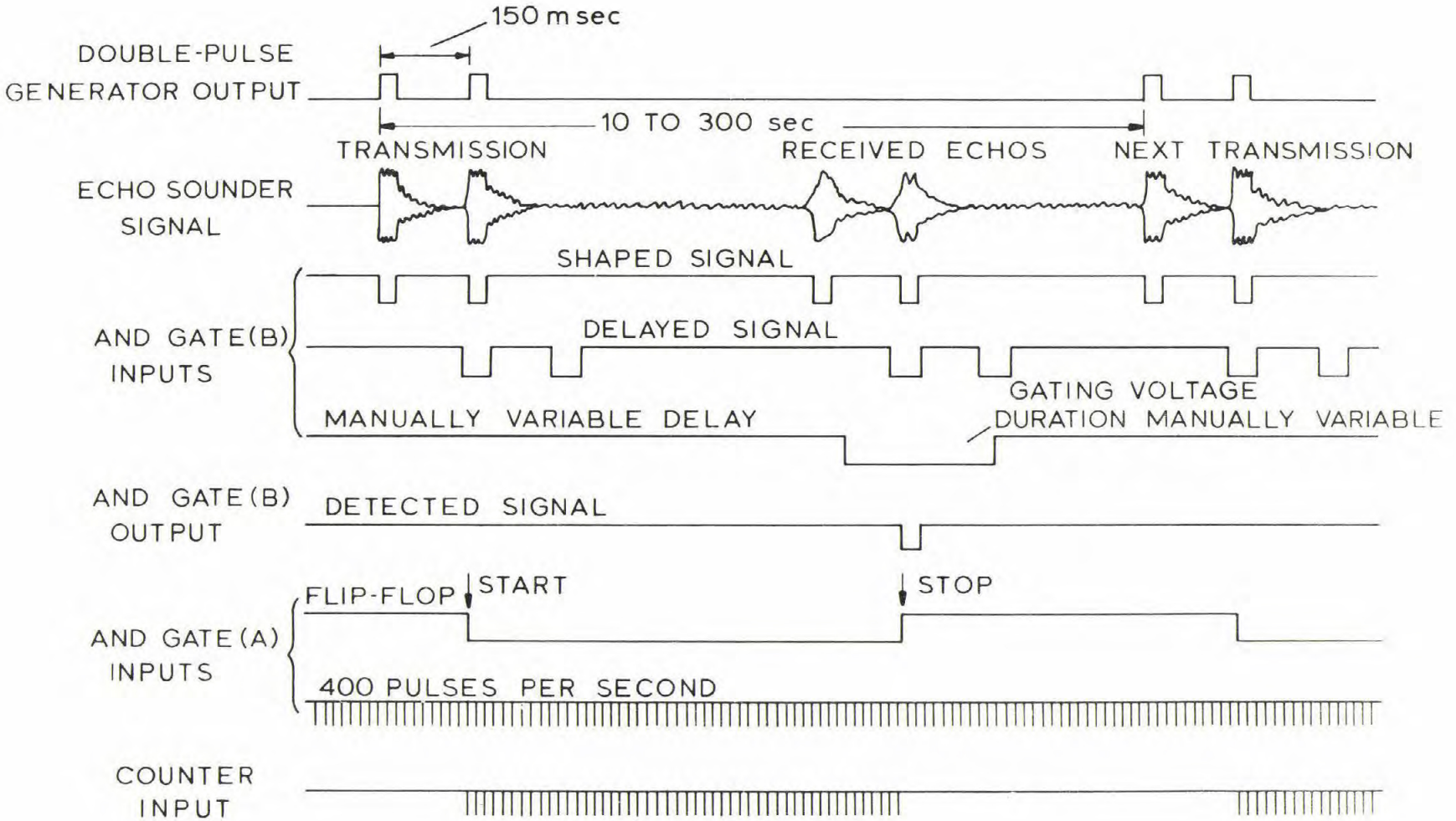


FIG. 2 DIGITAL DEPTH RECORDER – SOME WAVEFORMS

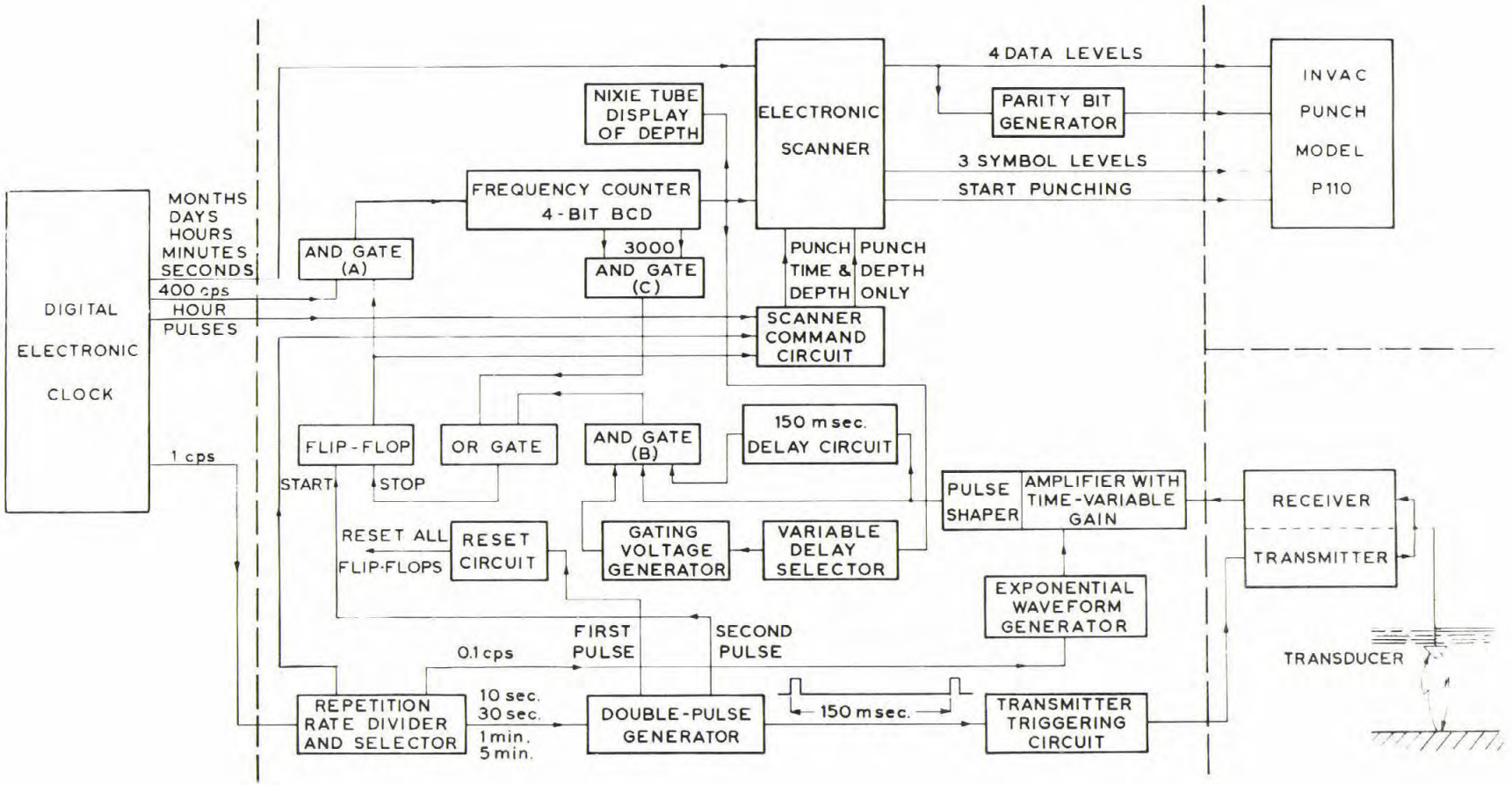


FIG. 3 DETAILED BLOCK DIAGRAM OF DIGITAL DEPTH RECORDER

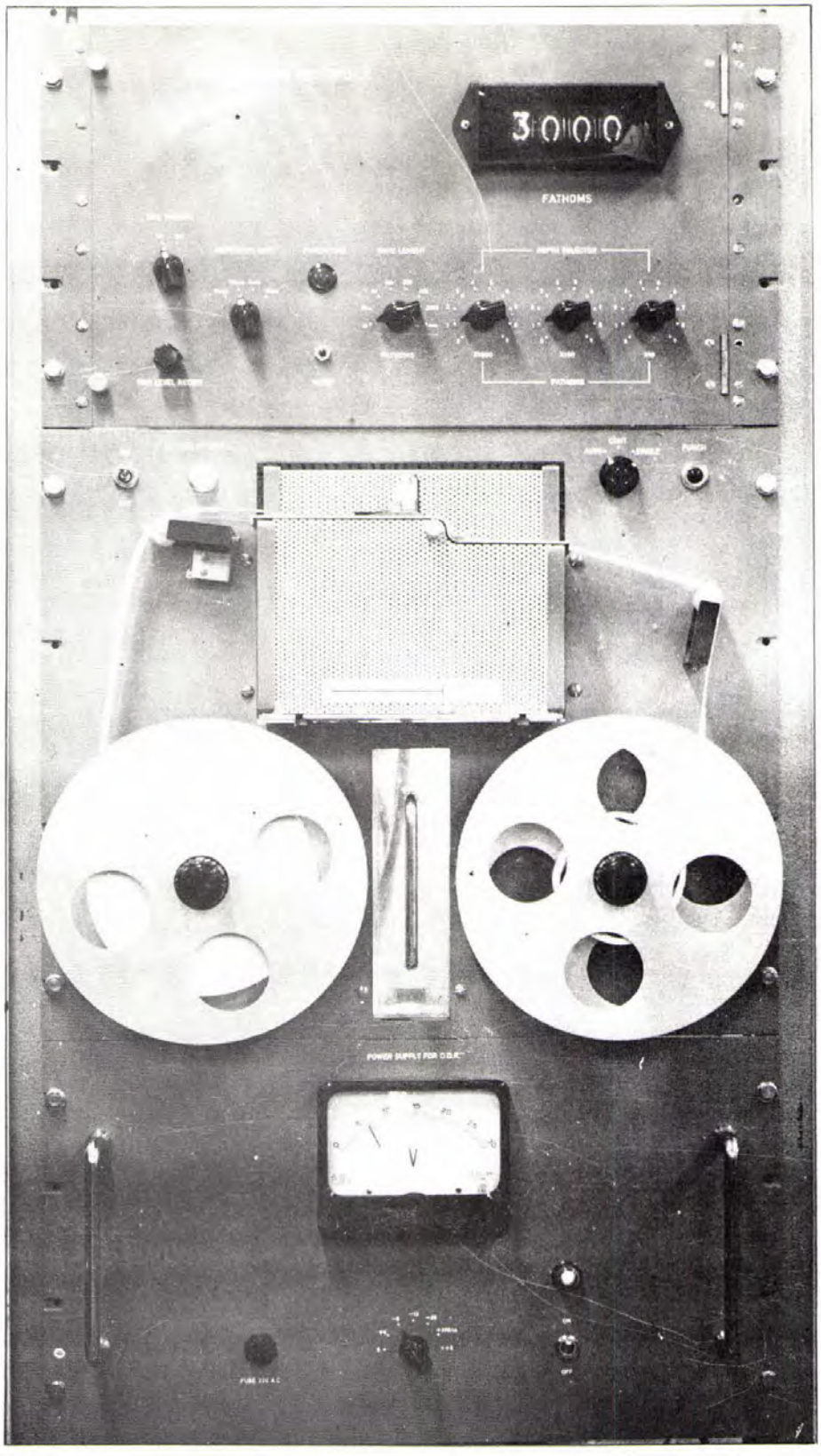
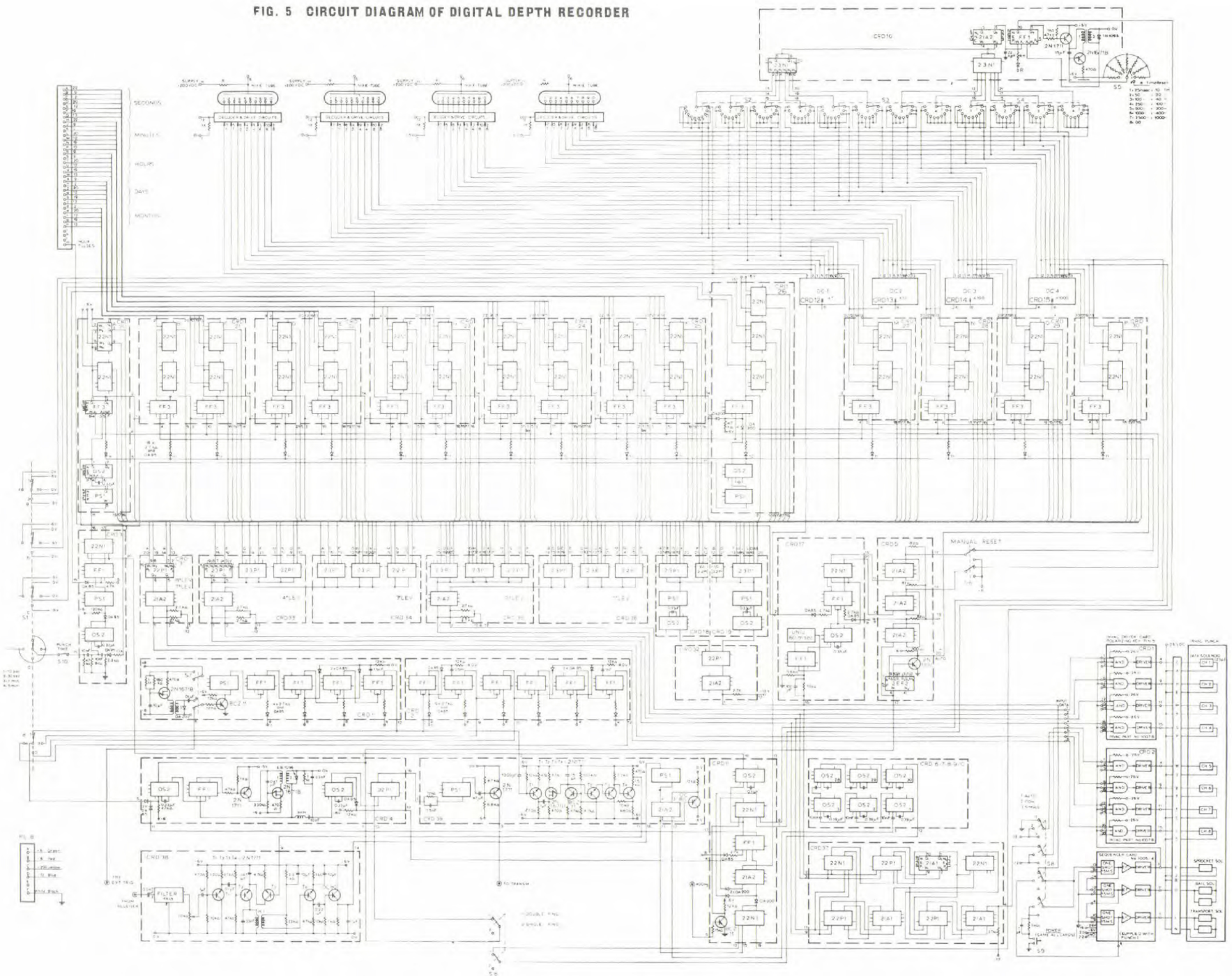


FIG. 4 PHOTOGRAPH OF DIGITAL DEPTH RECORDER

FIG. 5 CIRCUIT DIAGRAM OF DIGITAL DEPTH RECORDER



APPENDIX

The following punch code has been used:

Code	Significance
11100100	Time reading symbol
11100001	Repetition Rate 10 seconds
11100010	" " 30 "
11110101	" " 1 minute
11110110	" " 5 "
00110000	0
00100001	1
00100010	2
00110011	3
00100100	4
00110101	5
00110110	6
00100111	7
00101000	8
00111001	9

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